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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,755	09/26/2003	Echere Iroaga	1847-US	9347

7590 01/13/2005

Legal Department
Teradyne, Inc.
321 Harrison Avenue
Boston, MA 02118

EXAMINER
WELLS, KENNETH B

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,755	IROAGA, ECHERE	
	Examiner	Art Unit	
	Kenneth B. Wells	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *15-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance: See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Applicant's election of invention I, claims 1-14 is acknowledged. Claims 15-19 are therefore withdrawn from consideration by the examiner.

2. The drawings are objected to because In Fig. 4, FETs QP2, QPN should be shown with their gates connected to the output node of element 52, instead of just floating, as currently indicated.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet"

in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1, 9 and 14, it is not clear if the "current mirror circuit" on line 1 is part of the claimed invention, or if it is merely the intended use of the claimed compensation circuit. In other words, it cannot be determined in instant Fig. 4, which elements are being claimed, and which are the intended use. Is the recited first current mirror stage part of the claimed invention (i.e., part of the current compensation circuit)? Is the recited second current mirror stage part of the claimed invention (i.e., part of the current compensation circuit)? Applicant needs to clearly identify which elements in

instant Fig. 4 form the current compensation circuit and which form the current mirror recited on line 1 of claim 1. Also in claim 1, it is confusing to recite a path defined by a first mirror stage driving a second mirror stage. In the semiconductor art, "paths" are best defined in terms of where current flows (e.g., from a first node to a second node, through a first element, etc).

As a minor point, on line 4 of claim 5, a period is needed at the end of the line. In claim 8, there is no antecedent basis for the recited arrays of transistors. In claims 12 and 13, there is no antecedent basis for "the range of available compensation current" and "the common source stage".

4.The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5, 9-11 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Pricer et al.

Note Fig. 1B, where the recited impedance divider reads on the combination of resistors 18, 20, 22' and 26; the recited supply voltage is the voltage across these resistors; and the recited gain stage is the combination of FETs 14a and 14b. The recited output node of the impedance divider is between resistors 20 and 26. The recited current mirror circuit (line 1 of claim 1) and the recited first and second current mirror stages (lines 2-3) are considered as intended use and thus not accorded patentable weight for defining over the applied prior art. Note that the sources of FETs 14a and 14b are in common (claims 2 and 11). The return voltage source of claim 5 is ground.

5. Claims 1, 2, 5 and 9-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang.

Note Fig. 6, where the recited impedance divider reads on the combination of resistors 40 and 42; the recited supply voltage is the voltage across these resistors; and the recited gain stage is the combination of FETs 46, 50 with resistor 44 and amplifier 48. The recited output node of the impedance divider is between resistors 40 and 42. The recited current mirror circuit (line 1 of claim 1) and

the recited first and second current mirror stages (lines 2-3) are considered as intended use and thus not accorded patentable weight for defining over the applied prior art. Note that the sources of FETs 40 and 42 are in common (claims 2 and 11). The return voltage source of claim 5 is ground. The recited means for setting the compensation current from the current source and/or the gain of the common source FETs 46, 50 (claims 12 and 13) reads on amplifier 48.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pricer et al or Wang.

Though not specifically stated by the references, forming the Fig. 1B circuit on a single IC would have been obvious to of ordinary skill in the art who knows the

advantages of this (e.g., all circuit elements will have similar response characteristics, etc).

7. Claims 3, 4, 8, 12 and 13 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Note Fig. 6 of Galipeau, Fig. 5 of Nomura et al and Fig. 2 of Nishiwaki et al.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757. The examiner can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached at (571)272-1740. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kenneth B Wells/
Kenneth B. Wells
Primary Examiner
Art Unit 2816

January 10, 2005